CLAIMS

What is claimed is:

1. A complementary metal-oxide semiconductor (CMOS) output buffer comprising:

a pre-driver logic, comprising a clock input, an enable, a first output, a second output, a positive power input, and a negative power input;

a first inverter, comprising a first inverter input and a first inverter output;

a second inverter, comprising a second inverter input and a second inverter output;

a nand gate, comprising a first nand gate input, a second nand gate input, and a nand gate output;

a nor gate, comprising a first nor gate input, a second nor gate input, and a nor gate output;

a first comparator, comprising a first comparator positive input, a first comparator negative input, and a first comparator output;

a second comparator, comprising a second comparator positive input, a second comparator negative input, and a second comparator output;

a resistance, comprising a first end and a second end;

a p-channel metal-oxide semiconductor (PMOS), comprising a PMOS gate, a PMOS source, and a PMOS drain; and

an n-channel metal oxide semiconductor (NMOS), comprising an NMOS

gate, an NMOS source, and an NMOS drain;

whereby, the first output of the pre-driver logic is coupled to the first inverter input and the first inverter output is coupled to the first nand gate input and the second output of the pre-driver logic is coupled to the second inverter input and the second inverter output is coupled to the first nor gate input;

whereby, the second nand gate input is coupled to the first comparator output and the second nor gate input is coupled to the second comparator output;

whereby, the nand gate output is coupled to the PMOS gate and the nor gate output is coupled to the NMOS gate;

whereby, the PMOS source and the positive power input are coupled to a first positive power supply and the NMOS source and the negative power input are coupled to a first negative power supply;

whereby, the PMOS drain, NMOS drain, and the first end of the resistance are coupled;

whereby, the second end of the resistor, the first comparator negative input, and the second comparator negative input are coupled;

whereby, the first comparator positive input is coupled to a second positive power supply and the second comparator positive input is coupled to a second negative power supply; and

whereby, the second positive power supply is less than the first positive power supply and the second negative power supply is less than the first

negative power supply.

2. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 1, whereby the first comparator and the second comparator are Schmitt triggers.

3. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 1, whereby a maximum voltage level of an output waveform of the output buffer is less than a maximum voltage level of the first positive power supply.

4. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 1, whereby a minimum voltage level of an output waveform of the output buffer is greater than a minimum voltage level of the first negative power supply.

5. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 1, whereby a minimum voltage level of an output waveform of the output buffer is greater than zero volts.

6. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 1, whereby a duty cycle of an output waveform of the output buffer is equal to a duty cycle of the clock input.

7. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 1, whereby when charging a load coupled to the output buffer, the first comparator maintains the PMOS open while a maximum voltage level of an output waveform of the output buffer is less than a voltage level of the second positive power supply.

8. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 7, whereby when the maximum voltage level of the output waveform equals the voltage level of the second positive power supply, the output buffer is tri-stated.

9. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 1, whereby when discharging a load coupled to the output buffer, the second comparator maintains the NMOS open while a minimum voltage level of an output waveform of the output buffer is greater than a voltage level of the second negative power supply.

10. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 9, whereby when the minimum voltage level of the output waveform equals the voltage level of the second negative power supply, the output buffer is tri-stated.

11. A complementary metal-oxide semiconductor (CMOS) output buffer comprising:

a pre-driver logic, comprising a clock input, an enable, a first output, a second output, a positive power input, and a negative power input;

a first inverter, comprising a first inverter input and a first inverter output;

a second inverter, comprising a second inverter input and a second inverter output;

a nand gate, comprising a first nand gate input, a second nand gate input, and a nand gate output;

a nor gate, comprising a first nor gate input, a second nor gate input, and a nor gate output;

a first comparator, comprising a first comparator positive input, a first comparator negative input, and a first comparator output;

a second comparator, comprising a second comparator positive input, a second comparator negative input, and a second comparator output;

a resistance, comprising a first end and a second end;

a p-channel metal-oxide semiconductor (PMOS), comprising a PMOS gate, a PMOS source, and a PMOS drain; and

an n-channel metal oxide semiconductor (NMOS), comprising an NMOS gate, an NMOS source, and an NMOS drain;

whereby, the first output of the pre-driver logic is coupled to the first inverter input and the first inverter output is coupled to the first nand gate input and the second output of the pre-driver logic is coupled to the second inverter input and the second inverter output is coupled to the first nor gate input;

whereby, the second nand gate input is coupled to the first comparator output and the second nor gate input is coupled to the second comparator output;

whereby, the nand gate output is coupled to the PMOS gate and the nor gate output is coupled to the NMOS gate;

whereby, the PMOS source and the positive power input are coupled to a first positive power supply and the NMOS source and the negative power input are coupled to a first negative power supply;

whereby, the PMOS drain, NMOS drain, and the first end of the resistance are coupled;

whereby, the second end of the resistor, the first comparator negative input, and the second comparator negative input are coupled; and

whereby, the first comparator positive input is coupled to a second positive power supply and the second comparator positive input is coupled to a second negative power supply.

12. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 11, whereby the second positive power supply is less than the first

positive power supply and the second negative power supply is less than the first negative power supply.

13. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 11, whereby the first comparator and the second comparator are Schmitt triggers.

14. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 11, whereby a maximum voltage level of an output waveform of the output buffer is less than a maximum voltage level of the first positive power.

15. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 11, whereby a minimum voltage level of an output waveform of the output buffer is greater than a minimum voltage level of the first negative power supply.

16. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 11, whereby a minimum voltage level of an output waveform of the output buffer is greater than zero volts.

17. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 11, whereby a duty cycle of an output waveform of the output buffer is equal to a duty cycle of the clock input.

18. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 11, whereby when charging a load coupled to the output buffer, the first comparator maintains the PMOS open while a maximum voltage level of an output waveform of the output buffer is less than a voltage level of the second positive power supply.

19. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 18, whereby when the maximum voltage level of the output waveform equals the voltage level of the second positive power supply, the output buffer is tri-stated.

20. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 11, whereby when discharging a load coupled to the output buffer, the second comparator maintains the NMOS open while a minimum voltage level of an output waveform of the output buffer is greater than a voltage level of the second negative power supply.

21. The complementary metal-oxide semiconductor (CMOS) output buffer of claim 20, whereby when the minimum voltage level of the output waveform equals the voltage level of the second negative power supply, the output buffer is tri-stated.

22. A complementary metal-oxide semiconductor (CMOS) compatible circuit comprising:

a voltage-based output circuit, where by a full signal swing of an output of the voltage-based output circuit is prevented in order to reduce power consumption, reduce switching time, and reduce Electromagnetic Interference (EMI).

23. The complementary metal-oxide semiconductor (CMOS) compatible circuit of claim 22, whereby the voltage-based output circuit comprises an output buffer or a differential pair.

24. A output circuit, comprising:

a voltage-based output circuit, where by a full signal swing of an output of the voltage-based output circuit is prevented in order to reduce power consumption, reduce switching time, and reduce Electromagnetic Interference (EMI).

25. The output circuit of claim 24, whereby the voltage-based output circuit comprises an output buffer or a differential pair.

26. The output circuit of claim 24, whereby the voltage-based output circuit

is complementary metal-oxide semiconductor (CMOS) compatible.